UD info Corp.

Industrial PATA Solid State Drive
IFD-25UD Series
Product DataSheet

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Revision History

Revision	Draft Date	History	Author
1.0	2014/6/11	New release	Golden Lee
1.1	2014/11/11	Modify Partnumber decoder	Golden Lee

Product Overview

- **Capacity**
  - SLC: 4GB up to 256GB
  - MLC: 4GB up to 512GB
- **Standard ATA/IDE Bus Interface**
  - 512 Bytes/ Sector
  - ATA command set compatible
- **Flash Interface**
  - Flash Type: SLC,MLC
- **Performance**
  - Read: up to 80 MB/s
  - Write: up to 90 MB/s
- **Power Consumption**[Note1]
  - Active mode: < 945mW
  - Idle mode: < 52mW
- **TBW (Terabyte Written)**
  - SLC: 2697 TBW for 256GB
  - MLC: 267 TBW for 512GB
- **MTBF**
  - SLC: 3,000,000 hours
  - MLC: 2,000,000 hours
  - pSLC: 2,500,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
- **Low Power Management**
  - Power Sleep Mode
- **Temperature Range**
  - Operation (Standard): 0°C ~ 70°C
  - Operation (Wide): -40°C ~ 85°C
  - Storage: -40°C ~ 85°C
- **Compliant**
  - RoHS
  - CE & FCC

Notes:

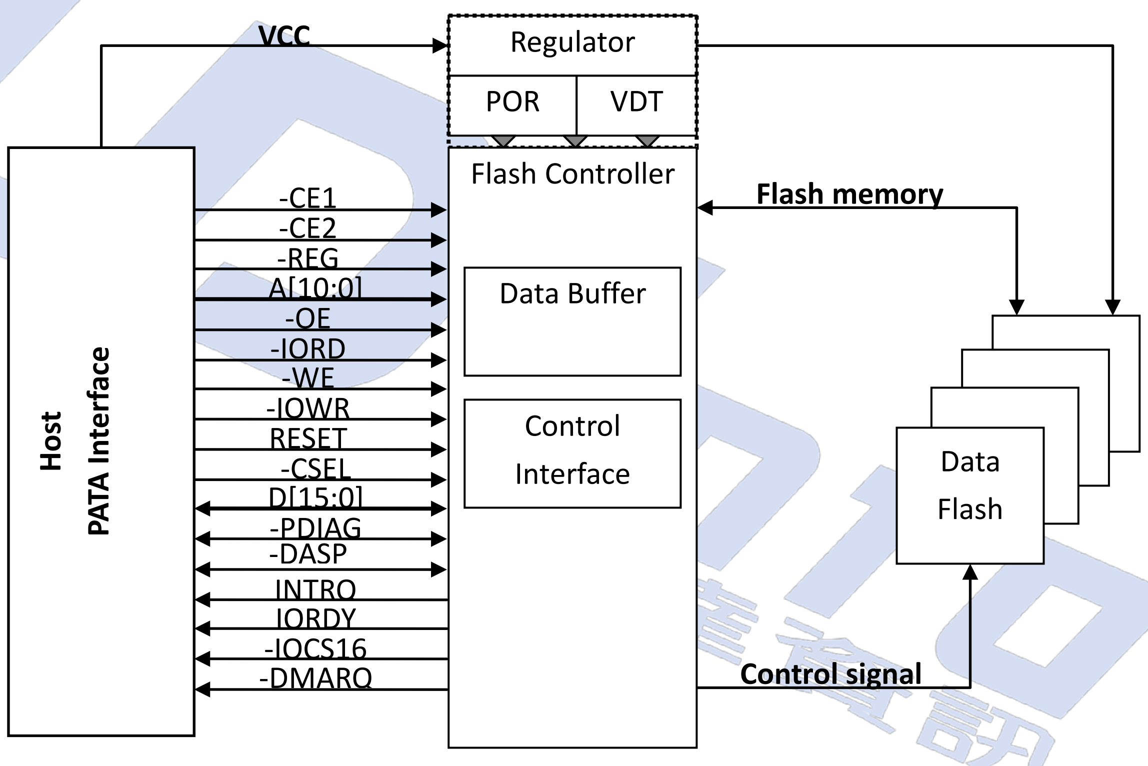
1. Please see Power Consumption” for details.

1. INTRODUCTION

1.1. General Description

UDinfo 2.5” PATA Solid State Disk (SSD) is a non-volatile, solid state data storage system, and has become a more popular storage media solution, compared to a conventional Hard Disk Drive (HDD). Due to lack of any mechanical components, SSD provides a more robust and cost effective storage solution for any embedded application. Since SSD comes with a standard ATA interface which is fully compatible with traditional HDD, designers will find 2.5” PATA SSD as an easy solution for integration in PC-based system.

1.2. Block Diagram



2.5” PATA Block Diagram

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - SLC: From 4GB up to 256GB
  - MLC: From 4GB up to 512GB
- **Standard 50-pin 2.5'' form factor**
- **Standard ATA/IDE Bus Interface**
  - 512 Bytes/Sector
  - Compatible with ATA command set
- **Data Transfer Mode:**
  - Support data transfer up to PIO mode 4
  - Support data transfer up to Multiword DMA mode 2
  - Support data transfer up to Ultra DMA mode 7
- **NAND Flash Interface**
  - Support SLC/MLC NAND flash memory
  - Support 16KB data per page NAND flash memory
- **ECC Scheme**
  - Up to 68 bits / 1K Byte
- **Intelligent ATA/IDE Module**
  - Built-in embedded flash file system
  - Implemented with both dynamic and static wear-leveling algorithms to increase endurance of flash media
- **Operating Voltage: 3.3V and 5.0V**
- **RoHS Compliance**
- **Power-saving implementation**
- **Support Static/Dynamic Wear Leveling function**
- **Light weight and noiseless**
- **Implemented with automatic error detection and retry capability**
- **Support power down commands and idle modes**

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational (Standard grade): 0°C to 70°C
  - Operational (Wide grade): -40°C to 85°C
- Humidity:
  - Standard grade: RH 90% under 40°C (operational)
  - Wide grade: RH 95% under 55°C (operational)

■ **High Temperature Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	70°C	0% RH	72 hours
Operation (Wide)	85°C	0% RH	72 hours
Storage (Standard)	85°C	0% RH	72 hours
Storage (Wide)	85°C	0% RH	168 hours

Result: No any abnormality is detected.

■ **Low Temperature Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	0°C	0% RH	72 hours
Operation (Wide)	-40°C	0% RH	72 hours
Storage (Standard)	-40°C	0% RH	72 hours
Storage (Wide)	-40°C	0% RH	168 hours

Result: No any abnormality is detected.

■ **High Humidity Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	40°C	93% RH	24 hours
Operation (Wide)	55°C	95% RH	72 hours
Storage (Standard)	40°C	95% RH	72 hours
Storage (Wide)	55°C	95% RH	96 hours

Result: No any abnormality is detected.

■ **Temperature Cycle Test**

	Temperature	Test Time	Cycle
Operation (Standard)	0°C	30 min	10 cycles
	70°C	30 min	
Operation (Wide)	-40°C	30 min	20 cycles
	85°C	30 min	
Storage (Standard)	-40°C	30 min	10 cycles
	85°C	30 min	
Storage (Wide)	-40°C	30 min	50 cycles
	85°C	30 min	

Result: No any abnormality is detected.

3.1.2. Shock

■ **Shock Specification**

	Acceleration Force	Half Sin Pulse Duration
Operational	1500G	0.5ms

Result: No any abnormality is detected when power on.

3.1.3. Vibration

■ **Vibration Specification**

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
Operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/60 min for each

Result: No any abnormality is detected when power on.

3.1.4. Drop

■ **Drop Specification**

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

Result: No any abnormality is detected when power on.

3.1.5. Bending

■ **Bending Specification**

	Force	Action
Non-operational	≥ 50N	Hold 1min/5times

Result: No any abnormality is detected when power on.

3.1.6. Torque

■ **Torque Specification**

	Force	Action
Non-operational	0.5N-m or 5 deg	Hold 1min/5times

Result: No any abnormality is detected when power on.

3.1.7. Electrostatic Discharge (ESD)

■ **Contact ESD Specification**

Device	Capacity	Temperature	Relative Humidity	+/- 4KV	Result
2.5” PATA SSD	64GB 128GB	24.0°C	49% (RH)	Device functions are affected, but EUT will be back to its normal or operational state automatically.	PASS

3.2. MTBF

MTBF, an acronym for Mean Time between Failures, is a measure of a device’s reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of UDinfo’s 2.5” PATA SSD is up to 3,000,000 hours.

3.3. Certification

- RoHS
- CE / FCC

3.4. Compliance

- Up to ATA/ATAPI-8 (Including S.M.A.R.T)

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Parameter	Rating
Operating Voltage	3.3V and 5V

4.2. Power Consumption

Current	Read	Write	Idle
SLC (max.)	490	510	17
MLC (max.)	1150	1500	52

Unit: mW

NOTES:

1. Samples were built using Toshiba NAND flash.
2. The operating voltage is 3.3V.
3. Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CyrstalDiskMark.
4. Power Consumption may vary from flash configuration or platform.

4.3. Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit	Remark
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
3	Ta	Operating Temperature	0	+70	°C	Commercial Grade
4	Tst	Storage Temperature	-25	+85	°C	Commercial Grade
5	Ta	Operating Temperature	-40	+85	°C	Industrial Grade
6	Tst	Storage Temperature	-40	+85	°C	Industrial Grade

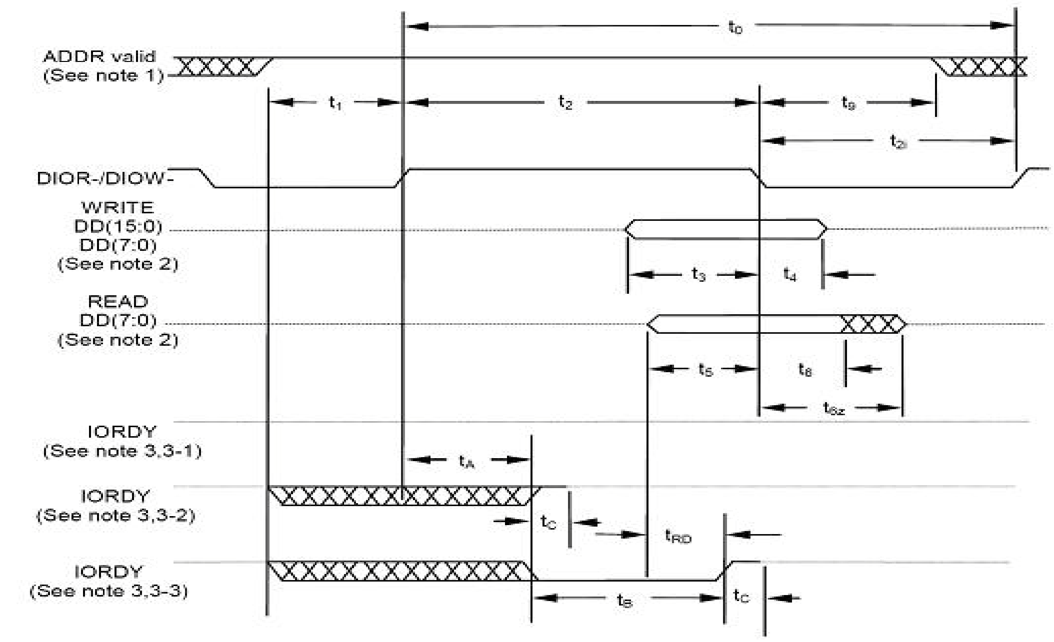
Parameter	Symbol	Min	TYP	MAX	Unit
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

4.4. DC Characteristics of 5.0V I/O Cells (Host Interface)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Vil	Input Low Voltage	TTL(5V)	--	--	0.85	V
Vih	Input High Voltage		1.25	--	--	V
Vil	Input Low Voltage	TTL(3.3V)	--	--	1.05	V
Vih	Input High Voltage		1.75	--	--	V
Vol	Output Low Voltage	|Iol| = 4~32 mA	--	--	0.4	V
Voh	Output High Voltage	|Ioh|= 4~32 mA	2.8	--	--	V
Iin	Input Leakage Current	No pull-up or pull down	-10	±1	10	µA
Ioz	Tri-state Output Leakage Current		-10	±1	10	µA

4.5. AC Characteristics

4.5.1. PIO Data Transfer



NOTES –
1 Device address consists of signals CS0-, CS1-, and DA(2:0)
2 Data consists of DD(7:0).
3 The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.
4 DMACK- shall remain negated during a register transfer.

PIO timing parameters		Mode 0 ns	Mode 1 ns	Mode2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time (min)	600	383	240	180	120	1,4
t_1	Address valid to DIOR-/DIOW- setup (min)	70	50	30	30	25	
t_2	DIOR-/DIOW- (min)	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW- recovery time (min)	--	--	--	70	25	1
t_3	DIOW- data setup (min)	60	45	30	30	20	
t_4	DIOW- data hold (min)	30	20	15	10	10	
t_5	DIOR- data setup (min)	50	35	20	20	20	
t_6	DIOR- data hold (min)	5	5	5	5	5	
t_{6z}	DIOR- data tristate (max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold (min)	20	15	10	10	10	10
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A) (min)	0	0	0	0	0	
t_A	IORDY Setup time	35	35	35	35	35	3
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release (max)	5	5	5	5	5	

Notes:

1. t_0 is minimum total cycle, t_2 is minimum DIOR-/DIOW- assertion time, and t_{2i} is the minimum DIOR-/DIOW- negation time. A host implementation shall lengthen t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any length host implementation.
2. This parameter specifies the time from the negation edge of DIOR- to the time that the data is released by the device.
3. The delay from the activation of FIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is complete. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, that t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then tRD shall be met and t_5 is not applicable.
4. Mode may be selected at the highest mode for the device if CS (1:0) and DA (2:0) do not change between read or write cycle or selects at the highest mode supported by the slowest device if CS (1:0) and DA (2:0) do change between read or write cycles.

4.5.2. IDE Interface Timing

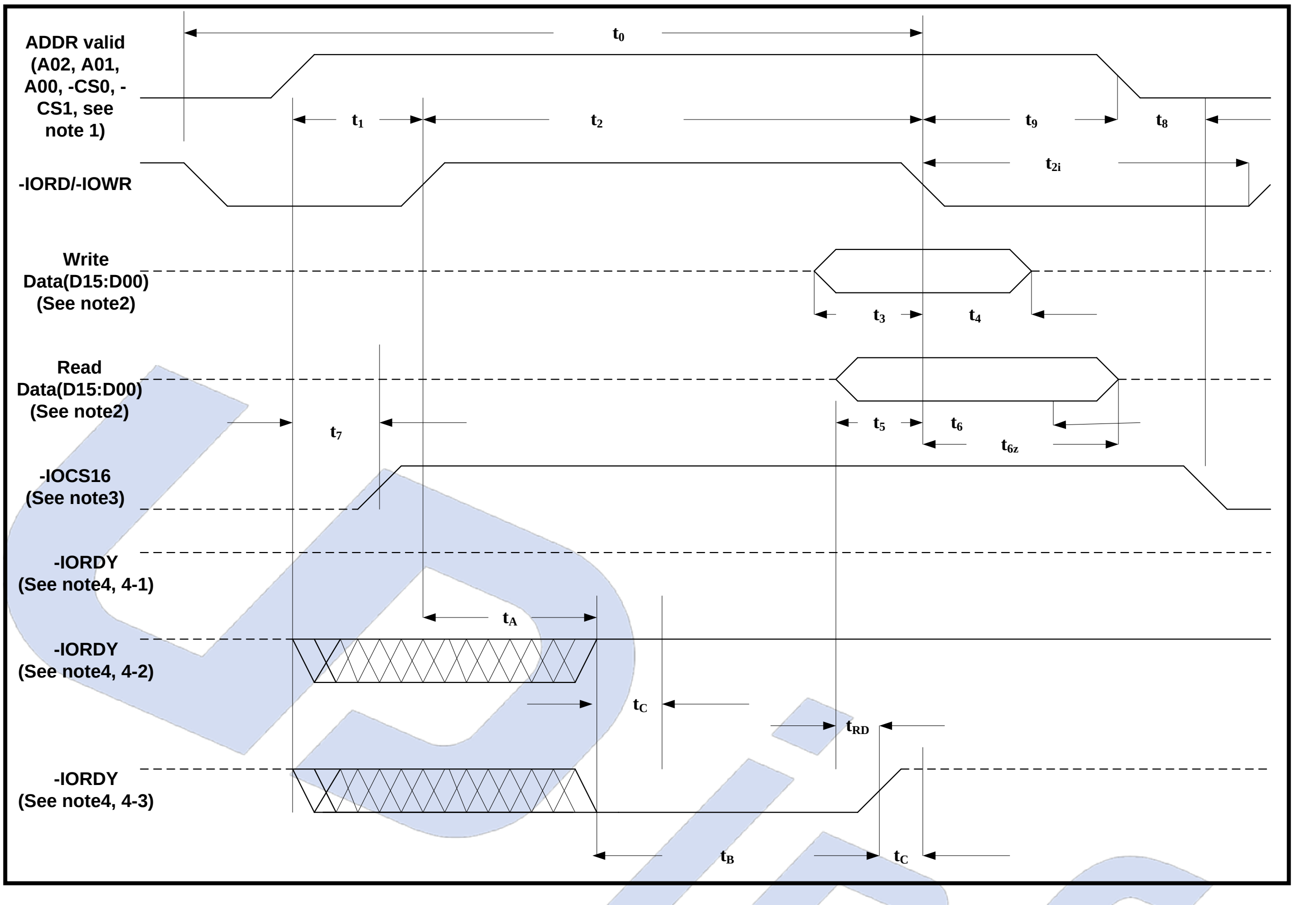


Figure 4-1 IDE Interface Timing (PIO Mode)

NOTES:

1. Device address consists of -CS0, -CS1, and A[02:00]
2. Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
3. -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
   - Device never negates IORDY: No wait is generated.
   - Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
   - Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

Table 4-1 IDE Interface Timing

Name	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data ho ld (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
T6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid ho ld	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially lo w after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na5	na5	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na5	na5	
tC	IORDY assertion to release (max)	5	5	5	5	5	na5	na5	

NOTES:

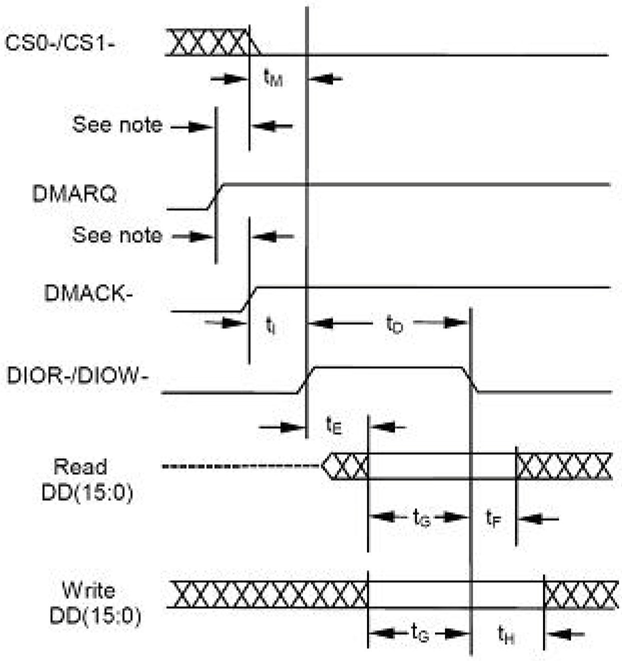
All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0nsec, but minimum -IORD width shall still be met.

1. t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0

is equal to or greater than the value reported in the device's identify device data. A PATA Storage Device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the PATA Storage Device (tri-state).
3. The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the PATA Storage Device is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the PATA Storage Device is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.
4. t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.
5. IORDY is not supported in this mode.

4.5.3. Multiword DMA Data Transfer



NOTE – The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

Figure 4-2 Initialing a Multiword DMA Data Burst

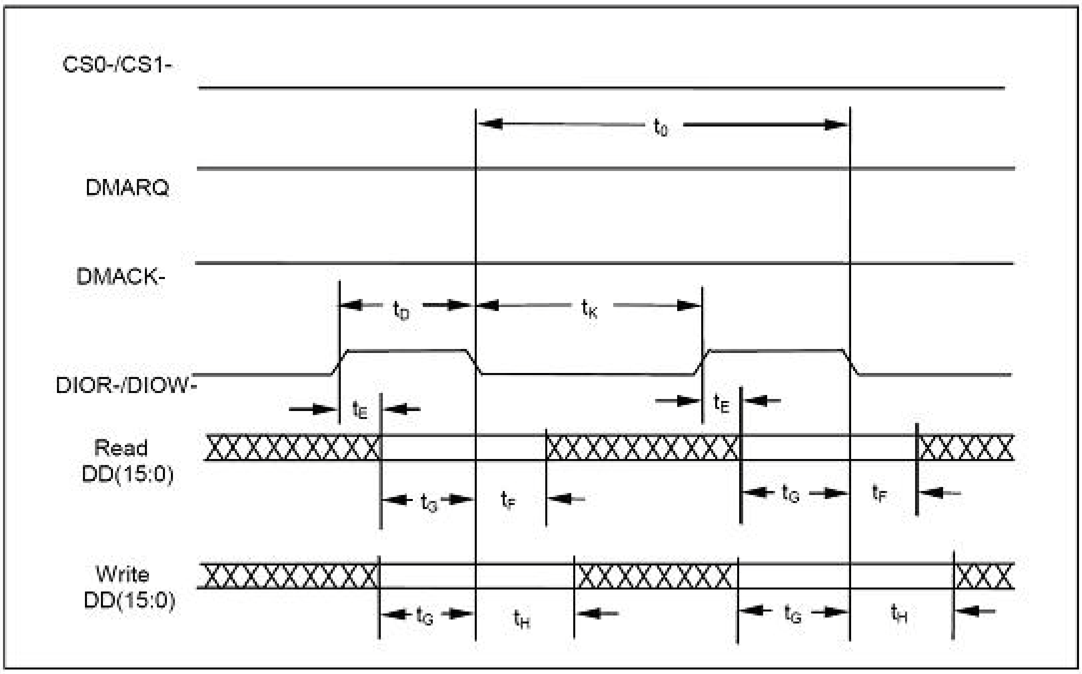
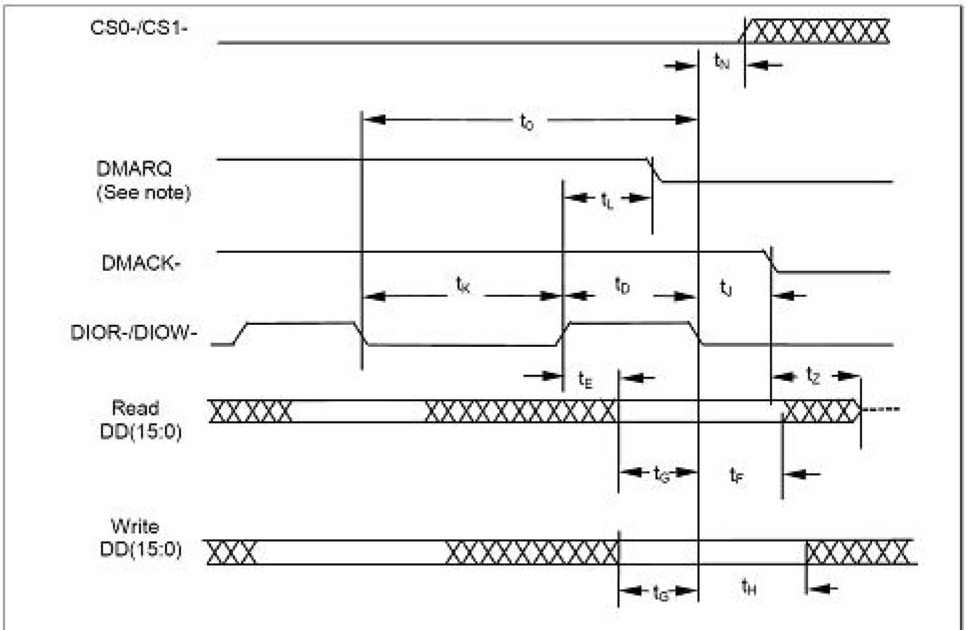


Figure 4-3 Sustaining a Multiword DMA Data Burst



NOTE – To terminate the data burst, the Device shall negate DMARQ within t_L of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation as shown in figure 66.

Figure 4-4 Device Terminating a Multiword DMA Data Burst

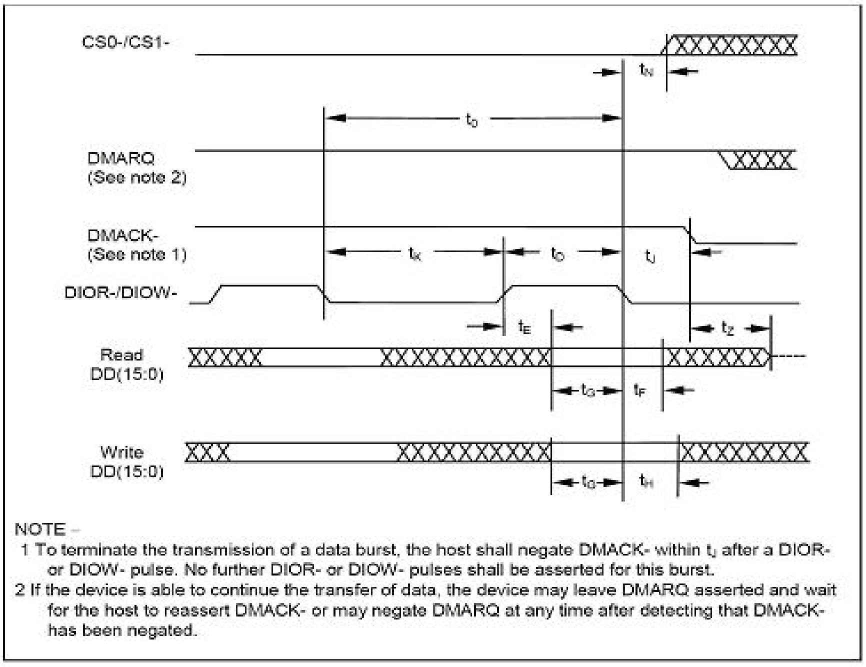


Figure 4-5 Host Terminating a Multiword DMA Data Burst

Multiword DMA timing parameters		Mode 0 ns	Mode 1 ns	Mode2 ns	Note
t_0	Cycle time (min)	480	150	120	See note
t_D	DIOR-/DIOW- asserted pulse width (min)	215	80	70	See note
t_E	DIOR- data access (max)	150	60	50	
t_F	DIOR- data hold (min)	5	5	5	
t_G	DIOR-/DIOW- data setup (min)	100	30	20	
t_H	DIOW- data hold (min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup (min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold (min)	20	5	5	
t_{KR}	DIOR- negated pulse width (min)	50	50	25	See note
t_{KW}	DIOW- negated pulse width (min)	215	50	25	See note
t_{LR}	DIOR- to DMACK delay (max)	120	40	35	
t_{LW}	DIOW- to DMACK delay (max)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW- (min)	50	30	25	
t_N	CS(1:0) hold (min)	15	10	10	
t_Z	DMACK- to read data released (max)	20	25	25	
Note: t_0 is the minimum total cycle. t_D is the minimum DIOR-/DIOW- assertion time, and t_K (t_{KR} or t_{KW}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.					

4.5.4. Ultra DMA Data Transfer

Ultra DMA data burst timing requirements

Name	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)		Mode 4 (in ns)		Mode 5 (in ns)		Mode 6 (in ns)		Measurement location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		Note 3
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	Note 4
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

NOTES –

1 All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2 All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and DMARDY- transitions are measured at the sender connector.

3 The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4 The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5 The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

Ultra DMA data burst timing descriptions

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge) (See note 2,5)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid) (See note 2,5)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge) (See note 3)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid) (See note 3)
t_{CS}	CRC word setup time at device (See note 2)
t_{CH}	CRC word hold time device (See note 2)
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK- negation) (See note 3)
t_{CVH}	CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid) (See note 3)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time (See note 1)
t_{MLI}	Interlock time with minimum (See note 1)
t_{UI}	Unlimited interlock time (See note 1)
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY (See note 4)
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

NOTES –

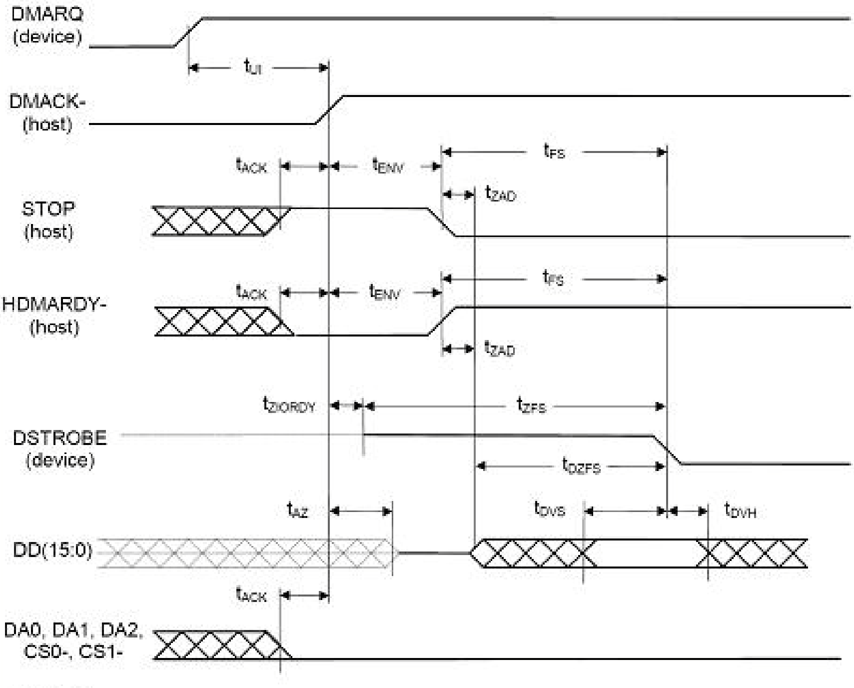
1 The parameters t_{UI}, t_{MLI} (in Figure 74 and Figure 75), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2 80-conductor cabling (See 7.3) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

3 Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

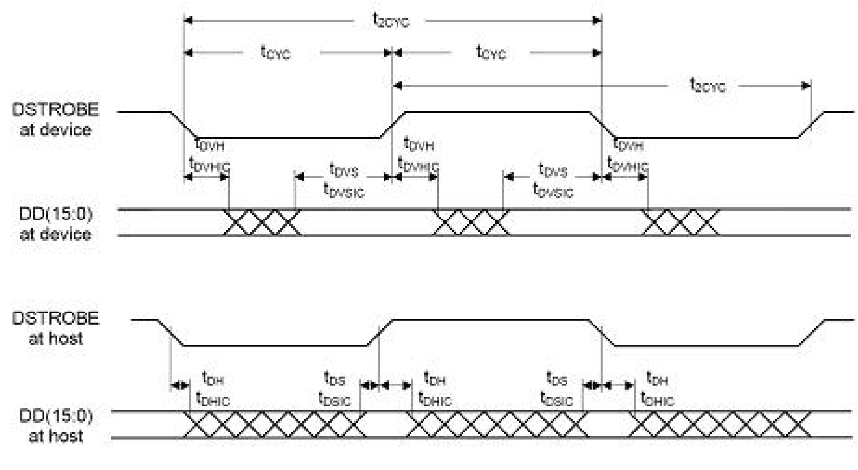
4 For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5 The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.



NOTES –
1 See 9.13.1 Initiating an Ultra DMA data-in burst.
2 The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 4-6 Initialing an Ultra DMA Data-in Burst



NOTES –
1 See 9.13.2 The data in transfer.
2 DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 4-7 Sustained Ultra DMA Data-in Burst

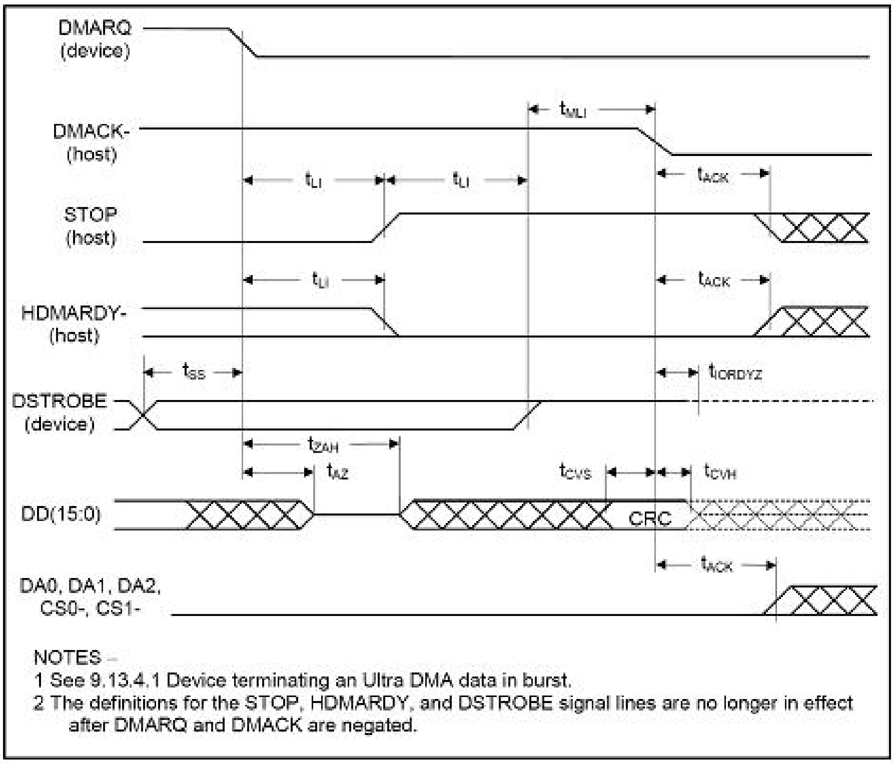


Figure 4-8 Device Terminating an Ultra DMA Data-in Burst

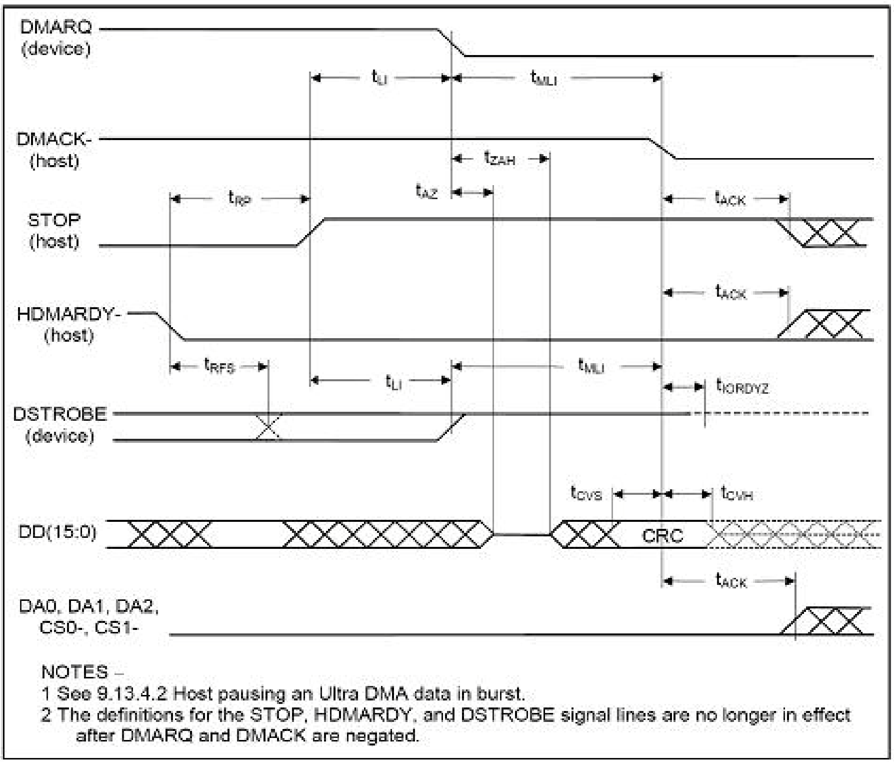


Figure 4-9 Host Terminating an Ultra DMA Data-in Burst

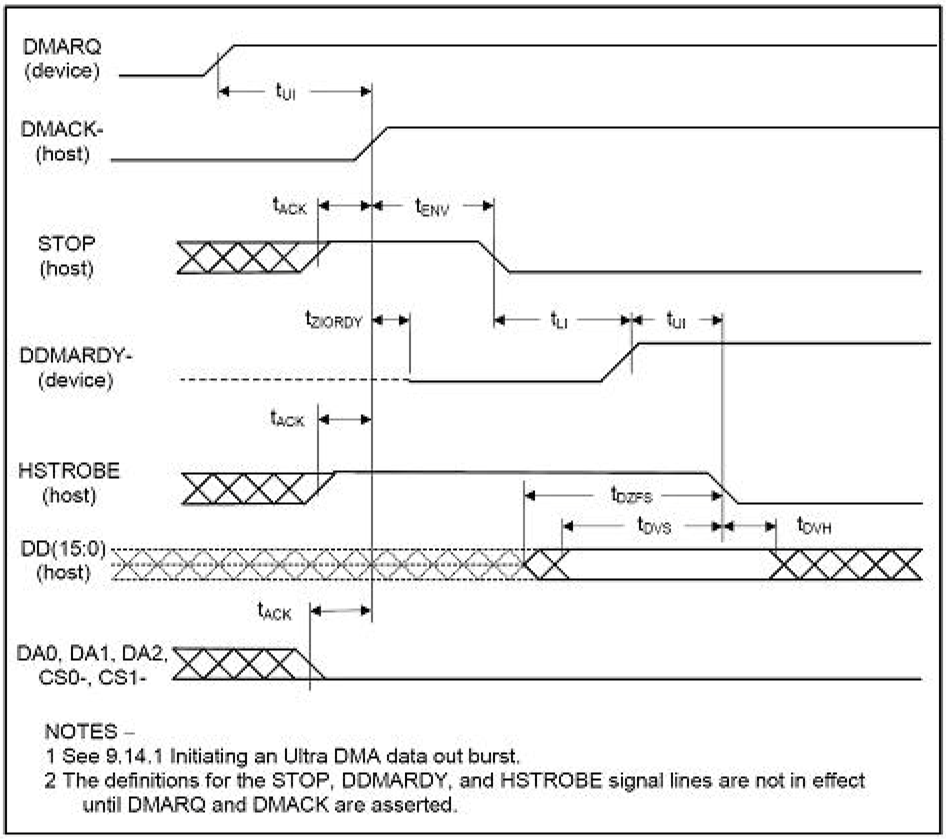


Figure 4-10 Initialing an Ultra DMA Data-out Burst

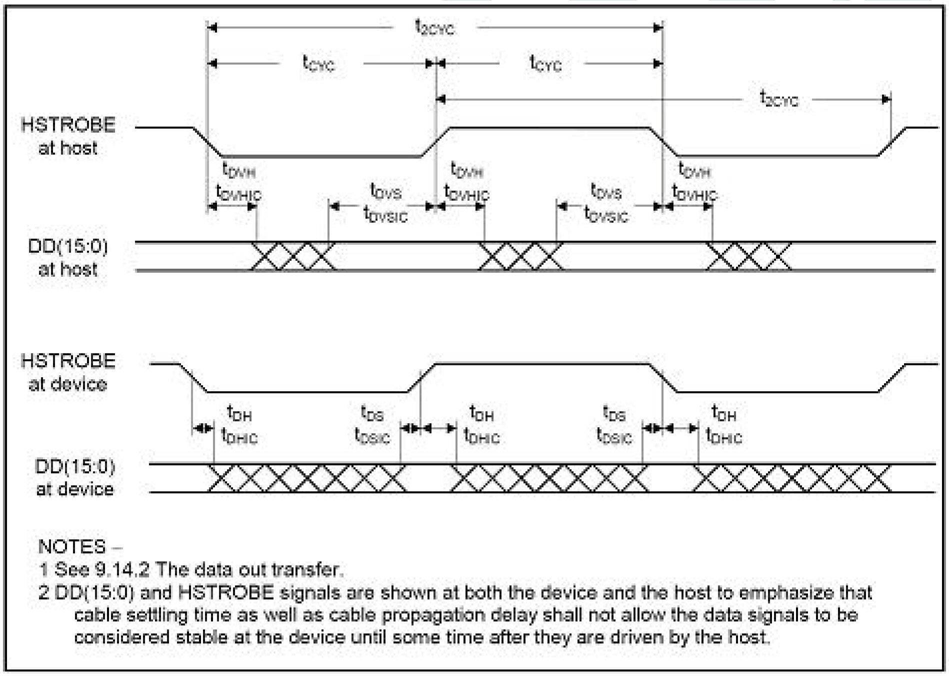


Figure 4-11 Sustained Ultra DMA Data-out Burst

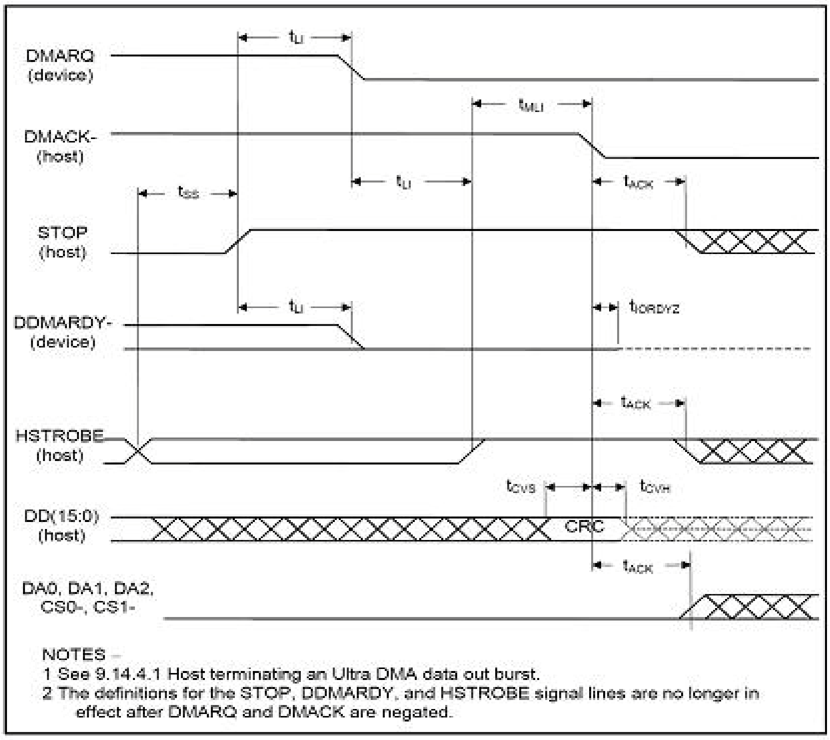


Figure 4-12 Host Terminating an Ultra DMA Data-out Burst

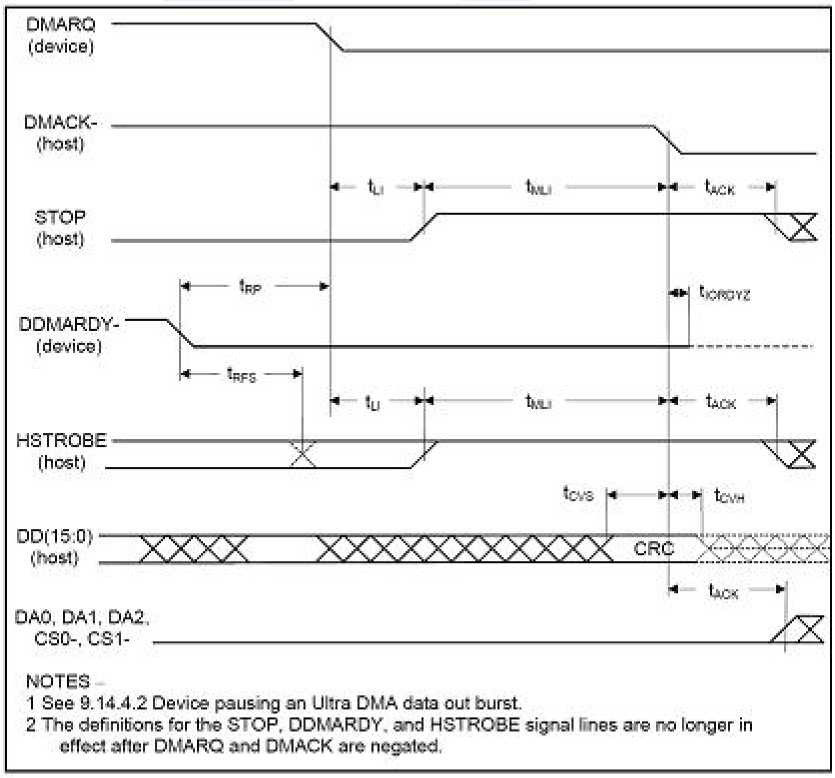


Figure 4-13 Device Terminating an Ultra DMA Data-out Burst

5. INTERFACE

5.1. Pin Assignment and Descriptions

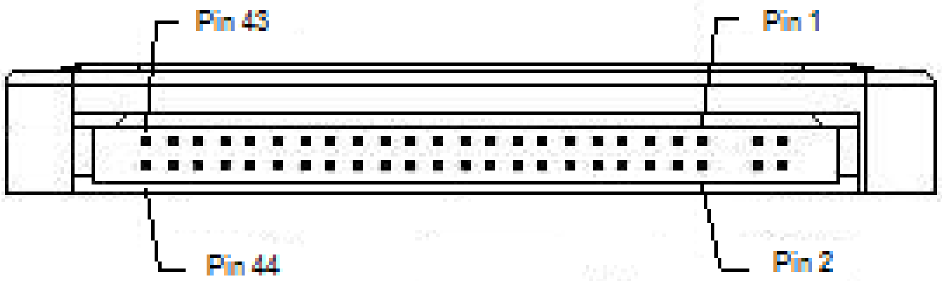


Table 5-1 2.5'' PATA SSD Pin Assignments

Pin	Pin Name	Pin	Pin Name
01	-RESET	02	GND
03	DD7	04	DD8
05	DD6	06	DD9
07	DD5	08	DD10
09	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	KEY_PIN(OPEN)
21	DMARQ	22	GND
23	-DIOW:STOP	24	GND
25	-DIOR:-HDMARDY:HSTOBE	26	GND
27	IORDY:DDMARDY:DSTROBE	28	CSEL
29	-DMACK	30	GND
31	INTRQ	32	IOIS16
33	DA1	34	-PDIAG:-CBLID
35	DA0	36	DA2
37	-CS0	38	-CS1
39	-DASP	40	GND
41	VCC	42	VCC
43	GND	44	NC

Table 5-2 2.5'' PATA SSD Pin Descriptions

Pin No.	Signal	I/O*	Description
01	-RESET	I	Hardware reset signal from the host
17,15,13,11,09,07, 05,03,04,06,08,10, 12,14,16,18	DD0~DD15(Device Data)	I/O	16-bit bi-direction Data Bus. DD (7:0) are used for 8-bit register transfers.
21	DMARQ(DMA Request)	O	For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.
23	-DIOW(I/O Write)	I	This is the strobe signal used by the host to write to the device register or Data port
	STOP(Stop UDMA Burst)		The host assert this signal during an UDMA burst to stop the DMA burst
25	IORDY(I/O channel ready)	O	This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.
	DDMARDY(UDMA ready)		The device will assert this signal to indicate that the device is ready to receive UDMA data-out burst.
	DSTROBE(UDMA data strobe)		When UDMA mode DMA Read is active, this signal is the data-in strobe generated by the device.
28	CSEL(Cable select)	I	This pin is used to configure this device as Device 0 or Device 1.
29	-DMACK(DMA acknowledge)	I	This signal is used by the host in respond to DMARQ to initiate DMA transfer.
31	INTRQ(Interrupt)	O	When this device is selected, this signal is the active high Interrupt Request to the host
32	IOIS16	O	During PIO transfer mode0,1or 2, this pin indicates to the host the 16-bit data port has been addressed and the device is prepared to send or receive a 16-bit data word. When transferring in DMA mode, the host must use a 16-bit DMA channel and this signal will not be asserted.
35, 33, 36	DA0~DA2(Device Address)	I	This is 3-bit binary coded Address Bus.
34	-PDIAG(Passed diagnostics)	I/O	This signal will be asserted by Device 1 to indicate

Pin No.	Signal	I/O*	Description
			to Device 0 that Device 1 has completed diagnostics,
	-CBLID(Cable assembly type identify)		
37, 38	-CS0, -CS1(Chip select)	I	These signals are used to select the Command Block and Control Block registers. When –DMACK is asserted, -Cs0 and –Cs1 shall be negated and transfers shall be 16-bit wide.
39	-DASP(Device active, Device 1 present)	I/O	During the reset protocol, -DASP shall be asserted by Device 1 to indicate that the device is present.
41, 42	VCC	P	Power supply
02, 19, 22, 24, 26, 30, 40, 43	GND	--	Ground.

Note:

“I”	An input from the host system to the device
“O”	An output from the device to the host system
“I/O”	An input/output (bi-direction) common
“P”	Power supply

6. SUPPORTED COMMANDS

6.1. ATA Task File Registers

The I/O decoding of each register is listed as follows:

-CS1	-CS0	A2	A1	A0	-DIOR=0 (-DIOW=1)	-DIOW=0 (-DIOR=1)
1	0	0	0	0	Data (Read)	Data (Write)
1	0	0	0	1	Error	Feature
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number (LBA7-0)	Sector Number (LBA7-0)
1	0	1	0	0	Cylinder Low (LBA 15-8)	Cylinder Low (LBA 15-8)
1	0	1	0	1	Cylinder High (LBA 23-16)	Cylinder High(LBA 23-16)
1	0	1	1	0	Drive/Head (LBA 27-24)	Drive/Head (LBA 27-24)
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

6.2. List of Command Sets

The table below summarizes the SSD command sets with the descriptions of individual command and task file for each command.

No.	Command Set	Code	FR	SC	SN	CY	DR	HD	LBA
1	CFA Erase Sector(s)	C0h	--	Y	Y	Y	Y	Y	Y
2	CFA Request Extended Error Code	03h	--	--	--	--	Y	--	--
3	CFA Translate Sector	87h	--	Y	Y	Y	Y	Y	Y
4	CFA Write Multiple w/o Erase	CDh	--	Y	Y	Y	Y	Y	Y
5	CFA Write Sector w/o Erase	38h	--	Y	Y	Y	Y	Y	Y
6	Check Power Mode	E5h	--	--	--	--	Y	--	--
7	Execute Device Diagnostic	90h	--	--	--	--	Y	--	--
8	Identify Device	ECh	--	--	--	--	Y	--	--
9	Idle	E3h	--	Y	--	--	Y	--	--
10	Idle Immediate	E1h	--	--	--	--	Y	--	--
11	Initialize Device Parameters	91h	--	Y	--	--	Y	Y	--
12	NOP	00h	--	--	--	--	Y	--	--
13	Read Buffer	E4h	--	--	--	--	Y	--	--
14	Read DMA	C8h	--	Y	Y	Y	Y	Y	Y
15	Read Multiple	C4h	--	Y	Y	Y	Y	Y	Y
16	Read Sector(s)	20h	--	Y	Y	Y	Y	Y	Y
17	Read Verify Sector(s)	40h	--	Y	Y	Y	Y	Y	Y
18	Seek	70	--	--	Y	Y	Y	Y	Y
19	Set Features	EFh	Y	--	--	--	Y	--	--
20	Set Multiple Mode	C6h	--	Y	--	--	Y	--	--
21	Sleep	E6h	--	--	--	--	Y	--	--
22	Standby	E2h	--	--	--	--	Y	--	--
23	Standby Immediate	E0h	--	--	--	--	Y	--	--
24	Write Buffer	E8h	--	--	--	--	Y	--	--
25	Write DMA	CAh	--	Y	Y	Y	Y	Y	Y
26	Write Multiple	C5h	--	Y	Y	Y	Y	Y	Y
27	Write Sector(s)	30h	--	Y	Y	Y	Y	Y	Y

Note:

FR: Feature Register
SC: Sector Count Register
SN: Sector Number Register
CY: Cylinder Low/High Register
DR: Drive bit of Drive/Head register
HD: Head No. of Drive/Head Register
LBA: LBA mode supported
Y: Set up
--: Not set up

6.3. Identify Drive Information

The Identity Drive Command enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration – bit significant for Non-removable device
1	xxxxh	2	Default number of cylinders
2	0000h	2	Reserved
3	xxxxh	2	Default number of heads
4	7E00h	2	Retired
5	0200h	2	Retired
6	xxxxh	2	Default number of sectors per track
7-8	xxxxh	4	Number of sectors per device
9	0000h	2	Retired
10-19	xxxxh	20	Serial Number in ASCII
20	0002h	2	Retired
21	0002h	2	Retired
22	0004h	2	Number of ECC Bytes passed on Read/Write Long Commands
23-26	Aaaah	8	Firmware revision in ASCII
27-46	xxxxh	40	Model number in ASCII
47	8001h	2	Maximum number of sector that shall be transferred on Read/Write Multiple commands
48	0000h	2	Reserved
49	2B00h	2	Capabilities-LBA/DMA Supported
50	4000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Retired
53	0007h	2	Word 54-58, 64-70 and 88 are valid
54	xxxxh	2	Current numbers of cylinders
55	xxxxh	2	Current numbers of heads
56	xxxxh	2	Current sectors per track
57-58	xxxxh	4	Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)

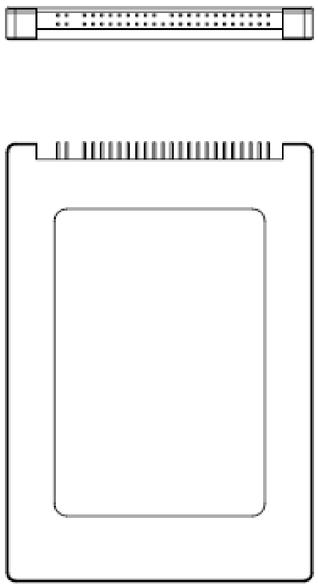
Word Address	Default Value	Total Bytes	Data Field Type Information
59	0101h	2	Multiple sector setting is valid
60-61	xxxxh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Retired
63	0007h	2	Multiword DMA mode 2 and below are supported
64	0003h	2	Advance PIO transfer modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time 120nsec
66	0078h	2	Manufacturer's recommended Multiword DMA transfer cycle time 120nsec
67	0078h	2	Minimum PIO transfer cycle time without flow control 120nsec
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control 120nsec
69-79	0000h	26	Reserved
80	0030h		Major version number
81	0000h		Reserved
82	7009h	2	Supports Security Mode feature set
83	5004h	2	Reserved
84	4000h		
85	7009h		Feature Setting
86	1004h		Feature Setting
87	4000h		Feature Setting
88	XXXXh	2	Ultra DMA mode 7 and below are supported, UDMA mode5 select
89-92	0000h	8	Reserved
93	xxxxh		
94-128	0000h	2	Enhanced security erase supported
129-159	0000h	62	Reserved vendor unique bytes
160-255	0000h	192	Reserved

Notes:

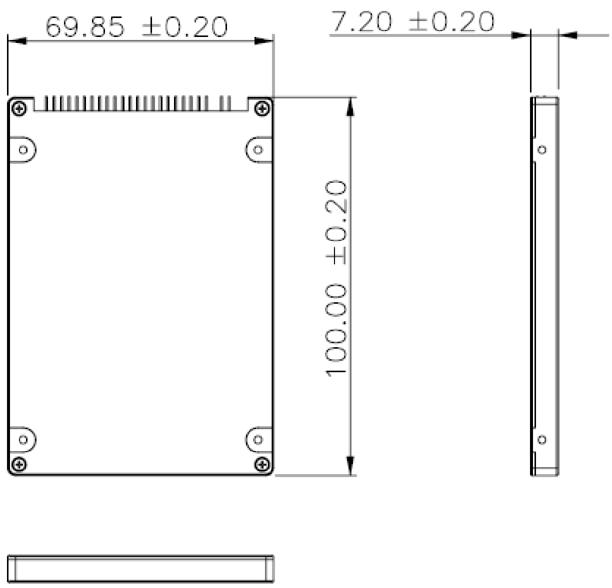
1. a = Vender Specific Configuration
2. n = Host Selectable Configuration

7. PHYSICAL DIMENSION

(Top view)



(Bottom view)



Unit: mm

8. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Term	Definitions
LBA	Logical block addressing
MB	Mega-byte
MTBF	Mean time between failures
PATA	Parallel advanced technology attachment
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk

9. BARCODE DESCRIPTION

IFD 25 U D 512 GBCAP

yymmddXX

Part Number

Manufacturing

Data: YYMMDD Flash Type:

10. PARTNUMBER DECODER

IFD-25UD$X^8X^9X^{10}X^{11}X^{12}X^{13}X^{14}X^{15}$ $X^{16}X^{17}$

$x^1x^2x^3$	x^4x^5	x^6x^7	x^8 x^9 x^{10} x^{11} x^{12}	x^{13}	x^{14}	x^{15}	$x^{16}x^{17}$
IFD	25	UD	004GB 064GB 008GB 128GB 016GB 256GB 032GB 512GB	C: SLC Standard (0ºC ~ +70ºC) I: SLC Industrial (-40ºC ~ +85ºC) K: MLC Standard (0ºC ~ +70ºC) M: MLC Industrial (-40ºC ~ +85ºC) P: pSLC Standard (0ºC ~ +70ºC) F: pSLC Industrial (-40ºC ~ +85ºC)	A: Auto Detect P: PIO / Fix mode Q: PIO / Removable Z: PIO / Auto Detect M: MWDMA / Fix mode N: MWDMA / Removable W: MWDMA / Auto Detect U: UDMA / Fix mode V: UDMA / Removable Y: UDMA / Auto Detect	P	blank